# DCC Industry Quality Metrics

These quality metrics represent typical industry practice, and are used in conjunction with the NMRA Standards and Recommended Practices for Conformance and Inspection testing.

1. DCC Wiring

1.1. Decoder Electromechanical Connection

Decoder circuit boards may contain an optional socket for the wiring harness. This socket / harness combination is currently manufactured by JST. The socket part number is S 9B-ZR-SM2-TF for the surface-mount version.
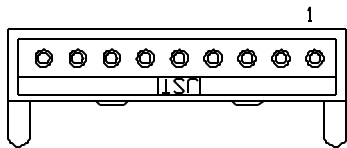
View looking into end of Decoder

Color	Use	Pin Number
Violet or Brown	Output 4	1
Black	Track –	2
Gray	Motor -	3
Yellow	Output 2 (Rear Headlight)	4
White	Output 1 (Front Headlight)	5
Blue	+V	6
Orange	Motor +	7
Red	Track +	8
Green	Output 3	9

1.2. Decoder Color Code of Wiring

RED — from right-hand rail power pick-up (or center rail, outside third rail, traction/overhead wire) to motor or interface

ORANGE — from interface to motor brush connected to right-hand rail (or center rail, outside third rail, traction wire)*

BLACK — from left-hand rail power pick-up to motor or interface

GRAY — from interface to motor brush connected to left-hand rail *

WHITE — front headlight(s) power sink

YELLOW — rear headlight(s) power sink

BLUE — common (+) headlight(s)/function(s) power source

BLACK with WHITE stripe — *OPTIONAL* common (-) power sink

GREEN — Output 1 power sink

VIOLET or BROWN — Output 2 power sink

2. DCC Communications

2.1. Baseline Packet Requirement Changes

The (former) baseline Speed and Direction Packets (14-Speed Steps) and the Extended Speed and Direction Packets (18-Speed Steps) have been reversed; 28-Speed Steps are required, and 28-Speed Steps are now

required. Digital Decoder Idle Packets and Digital Decoder Broadcast Stop Packets[1] (defined below) are optional for Command Stations, and required for decoders.

Speed and Direction Packet For Locomotive Decoders

111111111111 0	0AAAAAAA 0	01DCSSSS 0	EEEEEEEE 1
Preamble	Byte One	Byte Two	Byte Three (Error Detection Data Byte)

Byte One: Address Data Byte = 0AAAAAAA The address data byte contains the address of the intended recipient of the packet. Every Digital Decoder shall be capable of retaining and recognizing its own address for purposes of responding to Baseline Packets. Locomotive Digital Decoders shall support the full range of baseline addresses in such a manner that this address is easily configurable by the user[2]. It is acceptable for Digital Command Stations to restrict the number of valid addresses supported so long as this restriction is clearly and plainly labeled on the package and in the instructions.

Byte Two: Instruction Data Byte = 01DCSSSS The instruction data byte is a data byte used to transmit speed and direction information to the locomotive Digital Decoder.   Bits 0-3[3] provides 4 bits for speed (S) with bit 0 being the least significant speed bit. Bit four of byte 2 (C) by default, shall contain one additional speed bit which is the least significant speed bit. For backward compatibility, this bit may instead be used to control the headlight. This optional use is defined in RP-9.2.1. Bit 5 provides one bit for direction (D). When the direction bit (D) has a value of "1" the locomotive should move in the forward direction[4]. A direction bit with the value of "0" should cause the locomotive to go in the reverse direction. Bits 7 and 6 contain the bit sequence "01"[5] which are used to indicate that this instruction data byte is for speed and direction.

Byte Three: Error Detection Data Byte = EEEEEEEE The error detection data byte is a data byte used to detect the presence of transmission errors. The contents of the Error Detection Data Byte shall be the bitwise exclusive OR of the contents of the Address Data Byte and the Instruction Data Byte in the packet concerned. (e.g. the exclusive OR of bit 0 of the address data byte and bit 0 of the instruction data byte will be placed in bit 0 of the error detection data byte...) Digital Decoders receiving a Baseline Packet shall compare the received error detection data byte with the bitwise exclusive OR of the received address and instruction data bytes and ignore the contents of the packet if this comparison is not identical.

---

[1] Broadcast Stop Packet requirement for decoders, effective 1-Aug-2002.

[2] The Service Mode Recommended Practice (RP-9.2.3) contains one example of an acceptable method for user address configuration.

[3] Bits within a byte are numbered right to left with bit 0 (the right most bit) being the least significant bit and bit 7 (the left most bit) being the most significant bit.

[4] Forward in this case is in the direction of the front of the locomotive, as observed from the engineer's position within the locomotive.

[5] Other bit patterns in bits 7 and 6 are reserved for other types of instruction data, and are defined in the Extended Packet Format Recommended Practice (RP-9.2.1).

$CS_3S_2S_1S_0$	Speed	$CS_3S_2S_1S_0$	Speed	$CS_3S_2S_1S_0$	Speed	$CS_3S_2S_1S_0$	Speed
00000	Stop	00100	Step 5	01000	Step 13	01100	Step 21
10000	Stop (I)	10100	Step 6	11000	Step 14	11100	Step 22
00001	E-Stop*	00101	Step 7	01001	Step 15	01101	Step 23
10001	E-Stop* (I)	10101	Step 8	11001	Step 16	11101	Step 24
00010	Step 1	00110	Step 9	01010	Step 17	01110	Step 25
10010	Step 2	10110	Step 10	11010	Step 18	11110	Step 26
00011	**Step 3**	00111	Step 11	01011	Step 19	01111	Step 27
10011	Step 4	10111	Step 12	11011	Step 20	11111	Step 28

- *Digital Decoders shall immediately stop delivering power to the motor.
- (I) Direction bit may be ignored for directional sensitive functions. (Optional)

2.2. Digital Decoder Broadcast Stop Packets For All Decoders[6]

111111111111 0   00000000 0   01DC000S 0   EEEEEEEE   1

 Preamble   Byte One   Byte Two   Byte Three (Error Detection Data Byte)

A three byte packet, whose first byte contains eight "0"s, whose second byte contains a specific stop command and whose third and final byte contains an error byte that is identical to the second byte of the packet, is defined as a Digital Decoder Broadcast Stop Packet. Upon receiving this packet where bit zero of byte two (S) contains a value of "0", digital decoders intended to control a locomotive's motor shall bring the locomotive to a stop.

Upon receiving this packet where bit zero of byte two (S) contains a value of "1", digital decoders intended to control a locomotive's motor shall stop delivering energy to the motor. If bit four of byte 2 (C) contains a value of "1", the direction bit contained in bit five of byte 2 (D) may optionally be ignored for all direction sensitive functions.

2.3. Advanced Operations Instruction (001)

CCCCC = 11110: Restricted Speed Step Instruction - Instruction "11110" is used to restrict the maximum speed of a decoder. Bit 7 of the data byte is used to enable ('0') or disable ('1') restricted speed operation. Bits 0-5 of the Data byte are the Speed Steps defined in S-9.2[7].

---

[6]Broadcast Stop Packet requirement for decoders, effective 1-Aug-2002.

[7] In 128 speed step mode, the maximum restricted speed is scaled from 28 speed mode.

2.4. Function Group Two Instruction (101)[8]

This instruction has the format 1011DDDD

Up to 8 additional auxiliary functions (F5-F12) can be controlled by a Function Group Two instruction. Bit 4 defines the use of Bits 0-3. When bit 4 is '1',Bits 0-3 shall define the value of functions F5-F8 with function F5 being controlled by bit 0 and function F8 being controlled by bit 3. When bit 4 is '0',Bits 0-3 shall define the value of functions F9-F12 with function F9 being controlled by bit 0 and function F12 being controlled by bit 3. A value of "1" shall indicate that the function is "on" while a value of "0" shall indicate that the function is "off".

2.5. Extended Accessory Decoder Control Packet Format

This is an experimental packet. Its inclusion here is to encourage experimentation.
The Extended Accessory Decoder Control Packet is included for the purpose of transmitting aspect control to signal decoders or data bytes to more complex accessory decoders. Each signal head can display one aspect at a time. Control of two signal heads is included in each packet transmission.

{preamble} 0 10AAAAAA 0 0AAA0AA1 0 XXXXYYYY 0 EEEEEEEE 1

XXXX is for head one and YYYY is for head two. For specific uses of these bits please contact the NMRA DCC Coordinator or DCC Working Group Chair. Note: Bit pattern 1110 is illegal for XXXX.

2.6. Broadcast Command For Accessory Decoders

Broadcast Command for Basic Accessory Decoders

The format for the broadcast instruction is:

{preamble} 0 10111111 0 1000CDDD 0 EEEEEEEE 1

This packet shall be executed by all accessory decoders. CDDD is defined as specified in the paragraph on Basic Accessory Decoder Packet Format.

Broadcast Command for Extended Accessory Decoders

The format for the broadcast instruction is:

{preamble} 0 10111111 0 00000111 0 XXXXYYYY 0 EEEEEEEE 1

All extended accessory decoders must execute this packet. XXXXYYYY is defined as specified in the paragraph on Extended Accessory Decoder Packet Format.

2.7. Operations Mode Acknowledgment

The advanced acknowledgment mechanism as defined in RP-9.2.3 is the only valid acknowledgement in operations mode. Whenever an acknowledgment is requested, the decoder shall respond using this mechanism.

---

[8] Any function in this packet group may be directionally qualified.

3. DCC Configuration Variables

3.1. Configuration Variable 1 - Primary Address

The default value for this Configuration Variable is 3, if the decoder is not installed in a locomotive or other unit.

3.2. Configuration Variable 22 - Consist Address Active for FL and F9-F12

Bit 2 corresponds to F9, while Bit 5 corresponds to F12.

3.3. Configuration Variables 33-46 - Output Locations 1-14 for Functions FL(f), FL(r), and F1-F12

Contains a matrix indication of which function inputs control which *Digital Decoder* outputs. This allows the user to customize which outputs are controlled by which input commands. The outputs that Function FL(f) controls are indicated in CV #33, FL(r) in CV#34, F1 in CV #35, to F12 in CV#46. A value of "1" in each bit location indicates that the function controls that output. This allows a single function to control multiple outputs, or the same output to be controlled by multiple functions. CVs 33-37 control outputs 1-8. CVs 38-42 control outputs 4-11 CVs 43-46 control outputs 7-14. The defaults is that FL(f) controls output 1, FL(r) controls output 2, F1 controls output 3 to F12 controls output 14. The lowest numbered output is in the LSB of the CV, as shown in the table below.

CV	Description	Output msb													lsb
		14	13	12	11	10	9	8	7	6	5	4	3	2	1
33	Forward Headlight FL(f)														d
34	Reverse Headlight FL(r)													d	
35	Function 1												d		
36	Function 2											d			
37	Function 3										d				
38	Function 4									d					
39	Function 5								d						
40	Function 6							d							
41	Function 7						d								
42	Function 8					d									
43	Function 9				d										
44	Function 10			D											
45	Function 11		d												
46	Function 12	d													

Table 1: Output Position vs. CV (a 'd' indicates the default position)

3.4. Configuration Variable 513 - Decoder Address (LSB)

Contains the low-order address bits for Accessory Decoders. The high-order address bits are stored in CV521. Two types of Accessory Decoder addressing are supported: Decoder-Address and Output-Address. The type of decoder is specified in CV541, bit 6. Decoders using either type of addressing will respond to the same Accessory Decoder Control Packet when CV513 = 1 and CV521 = 0. The factory default value is 1.

(1) Decoder-Address: Contains the six least significant bits of the accessory decoder's address in bits 0-5. These bits are transmitted as bits 0-5 in the first byte of the accessory decoder packet. See RP-9.2.1 for more information.

(2) Output-Address: The user places the output address Contains the address value results from the following formula: Output Address modulus 256 (Output Address mod 256, Output Address % 256).

The values contained in CV513 and CV521 correspond to the bits in the Accessory Decoder packets as follows:

Accessory-Output = (CV513+(CV521*256)) - 1
Bits 0 & 1 of the Accessory-Output are transmitted as bits 1 & 2 of byte 2 of both Accessory Decoder Control Packets. Bits 2-7 of the Accessory-Output are transmitted as bits 0-5 of byte 1 of both Accessory Decoder Control Packets. The three least-significant bits of CV521 contain the ones-complement of bits 4-6 of both Accessory Decoder Control Packets (See RP-9.2.1 for more information on the Accessory Decoder Control Packets).

If an accessory decoder supports more than one sequential output the value in CV513 will be the first output in the series

3.5. Configuration Variable 521 - Decoder Address (MSB)

Contains the high-order address bits for Accessory Decoders. The low-order address bits are stored in CV513. Two types of Accessory Decoder addressing are supported: Decoder-Address and Output-Address. The type of decoder is specified in CV541, bit 6. Decoders using either type of addressing will respond to the same Accessory Decoder Control Packet when CV513 = 1 and CV521 = 0.The bits transmitted are the ones complement of the value in this CV. See RP-9.2.1 for more information on the Accessory Decoder Control Packets.

(1) Decoder-Address: Contains the three most significant bits of the accessory decoder's address in bits 0-2. These bits are transmitted as bits 4-6 in the second byte of the accessory decoder packet.

(2) Output-Address: Contains the address value results from the quotient of the following formula: Output Address divided by 256 (Output Address div 256, Output Address / 256).

See CV513 for an explanation of how to determine the contents of CV513 and CV521.

3.6. Configuration Variable 541 - Accessory Decoder Configurations Supported

Bits 0-4 = Reserved for future use.
Bit 5 = Decoder Type: '0' = Basic Accessory Decoder; '1' = Extended Accessory Decoder
Bit 6 = Addressing Method: '0'= Decoder Address method; '1' = Output Address method
Bit 7 = Accessory Decoder: = "0" Multifunction Decoder (See CV-29 for description of bit
   Assignments for bits 0-6), "1" = Accessory Decoder. If bit 7 = 1, then the decoder may
   ignore the two most-significant bits of the CV number in Service Mode only. Using this
   feature CV513 becomes CV1, etc. Decoders which perform the translation must clearly
   document the feature in their manual.
Note: If the decoder does not support a feature contained in this table, it must not allow the bit to be set
   improperly.

4. DCC Decoder Configuration (Service Mode)

4.1. Service Mode Environment

3) Service Mode operations should be performed in an environment with limited energy to prevent damage to decoders during programming. For the purposes of this RP, limited energy is defined as 250 mA, sustained for more than 100 ms. A programmer may further limit the energy via a current limiting resistor, if it is clearly documented that not all compatible DCC devices may be programmed by this programmer.

4.2. Basic Acknowledgment

Basic acknowledgment is defined by the Digital Decoder providing an increased load (positive-delta) on the programming track of at least 60 mA for 6 ms +/-1 ms . It is permissible to provide this increased load by applying power to the motor or other similar device controlled by the Digital Decoder.

4.3. Register Definitions for Accessory Decoders

Register	RRR Value	CVs for Accessory Decoders
1	000	Lower Address (CV #513)
2	001	Undefined, see Mfgs. Documentation
3	010	Undefined, see Mfgs. Documentation
4	011	Undefined, see Mfgs. Documentation
5	100	Undefined, see Mfgs. Documentation
6	101	Undefined, see Mfgs. Documentation
7	110	Version Number (CV #7)
8	111	Manufacturer ID (CV #520)

4.4. Decoder Factory Reset

From time to time it may be desirable to request that the decoder reprogram all its CVs to a factory default condition. The following command sequence[9] shall be used for this purpose. The packet sequence for this command is identical to the packet sequence specified for Service Mode Instruction Packets for Physical Register Addressing.
The instruction packets for Decoder Factory Reset are 3 byte packets of the format:

long-preamble 0 01111111 0 00001000 0 01110111 1

this Instruction Type causes a WRITE operation that instructs the decoder to return to a factory default condition.
Because the packet sequence in service mode provides insufficient time for the decoder to rewrite all its CVs, the actual reprogramming all the decoder's CVs will normally occur during each subsequent power on cycle until such time that all CVs have been returned to a factory default condition. A value of 255 will be placed in CV8 until such time that the decoder has successfully rewritten all CVs to their factory default condition.

---

[9] Several valid existing alternative means for achieving decoder factory reset are also in use. Manufacturers may continue to use these alternate means for performing factory decoder reset but are encouraged to also support the standard specified means for achieving this result.